Design and Implementation of Energy Efficient Code Converters

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***Abstract*—One of the major concern of power dissipation in CMOS circuits is charging and discharging of capacitor. The power dissipation can be reduced by restoring this energy back to the source instead of discharging. Adiabatic circuits are designed in such a way that the charging of capacitive node takes place very slowly. It is observed that by charging the capacitor slowly the energy requires is lesser than the faster charging method. Adiabatic circuits use this methods viz. slow charging and discharging of capacitor, and recycling of charge to minimize the power consumption. In this paper different code converters Binary to Gray (B2G), Gray to Binary (G2B) and Binary to Excess-1 (B2E1) are designed using ECRL and PFAL adiabatic logic techniques. The designed circuits are extensively simulated on mentor graphics tool using TSMC 180nm technology node. The simulation results indicate that the designed circuits achieves power saving in the range of 74–23% at the frequency range of 0.1-100 MHZ.**

Keywords- Adiabatic logic, ECRL, PFAL, Four phase power clock.

I. INTRODUCTION

The power consumption plays an important role in present day VLSI technology. To design any portable device the major concern is low power. To achieve low power devices the internal circuits are designed in such a way that they produce less power dissipation [1]. As the power dissipation is low the device withstands for a long period as a result the life time of the device increases.

The power dissipation in conventional CMOSdesign can be minimized by reducing the supply voltage, node capacitance value and switching activity [2]. But reducing these parameters may degrade the performance of the device. So an efficient low power technique other than CMOS is necessary to have less power dissipation compared with the CMOS. This work focuses on a novel energy efficient technique called adiabatic logic [3] which is based on energy recovery principle. In this technique instead of discharging the consumed energy, it is recycled back to the power supply thereby In order to reduce overall power consumption [4]. The code converters are majorly used in encoding and decoding processes for security purposes mainly in digital circuits. In order to achieve low power dissipation [4], [5]the code converters in this work are designed using adiabatic logic.The rest of the paper is organized as follows. Section II deals with working principle and power dissipation of conventional CMOS logic and adiabatic logic circuits. Section III describes implementation and Simulation of code converters. Results are presented in section IV. Conclusion is given in section V.

II. CONVENTIONAL CMOS AND ADIABATIC LOGIC

A. Conventional CMOS Logic

The CMOS inverter [6] consists of a pull-up and pull-down networks connected to a load capacitance C_L. The capacitancein this case models the fan-out of the output signal. The total stored charge at load capacitor was dissipated through the NMOS transistor to ground, during the discharge operation. E_{total} is the total energy consumption due to the charging and discharging, it can be expressed as

$$E_{total} = E_{charge} + E_{discharge} \quad (1)$$

$$= \frac{1}{2} C_L V_{DD}^2 + \frac{1}{2} C_L V_{DD}^2 \quad (2)$$

$$= C_L V_{DD}^2 \quad (3)$$

The amount of energy stored in C_L is found by integrating the power over time and is given by

$$E_{stored} = \frac{1}{2} C_L V_{DD}^2 \quad (4)$$

Here half of the energy stored in the capacitor will be discharged during the discharge cycle. In order to have more energy savings it is necessary to minimize the energy waste in transistor network. If the circuit is drawn with frequency f, and period T, the total power used in circuit is

$$P_{applied} = \frac{E_{applied}}{T} = \frac{C_L V_{DD}^2}{T} \quad (5)$$

To minimize the energy wastage during charging adiabatic circuits use constant current source and charging at a lower frequency. The above optimization can be calculated by minimizing function energy dissipation and current, yielding the dissipated energy is given by

$$E_{dissipated} = P\Delta T = \left(\frac{CV_{DD}}{\Delta T}\right)^2 R\Delta T \quad (6)$$

It is clear that if the charging time is infinitely long theoretically there will be no energy dissipated. But long charging times are impractical. The power loss can be reduced but by spreading the charging time, peak current. Adiabatic switching achieves this by replacing constant DC voltage supply with a time varying LC driver/oscillator to get constant charging current.

B. Adiabatic Logic

The word Adiabatic literally is a thermodynamic process which involves no energy exchange with the surrounding thus no loss of energy due to dissipation. Here to increase the energy efficiency the charge is restored back to the supply instead of dissipation. There are two types of Adiabatic logic families [7]

Fully Adiabatic Logic: - In these circuits all the charge on load capacitance is recovered and feedback to power supply. This makes these types of circuits slower and more complex to design. Pass Transistor Adiabatic Logic(PAL) and Split-Rail Charge Recovery Logic (SCRL) techniques are the popular fully adiabatic logic techniques.

Partial Adiabatic Logic: - This logic is also known as Quasi Adiabatic logic. In these circuits some charge on load capacitance is dissipated and some part of the energy is only being able to recover. Hence these circuits are easy to implement as compared to fully adiabatic logic. Efficient Charge Recovery Logic (ECRL) [7],and Positive Feedback Adiabatic Logic (PFAL) [7]are two popular quasi adiabatic logic techniques.

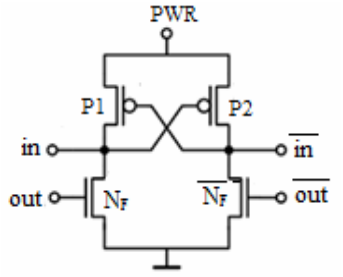

Fig.1. Basic ECRL inverter/buffer

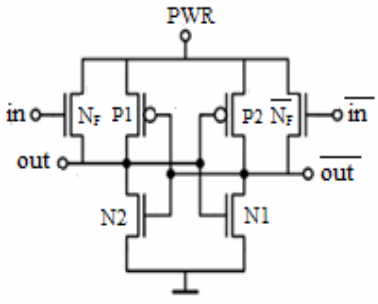

Fig.2. Basic PFAL inverter/buffer

The basic ECRL and PFAL buffer /inverter are shown figures 1 and 2 respectively. In both of the techniques to achieve slow charging process it uses a trapezoidal power supply voltage instead of constant DC voltage [8] as shown in figure 3.

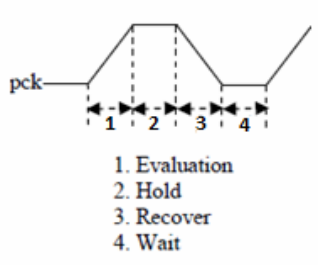

Fig.3. Phases in Adiabatic power supply

It has four intervals evaluate, Hold, Recover and Wait. In the evaluate interval, the outputs are evaluatedcorresponding to the inputs. During the hold interval, the outputs are maintained so as to be applied to the subsequent circuits. Then, in the recover interval, energy is recovered and transferred back to the power supply which is the main purpose of employing adiabatic logic. Finally to avoid the asymmetry, a wait interval is introduced.

III. IMPLEMENTATION AND CIRCUIT SIMULATION

The code converters are used in digital circuits for encoding and decoding processes. Some of the widely used code converters are Binary to Gray, Gray to Binary and Binary to Excess-1. These code converters are implemented using ECRL [9] and PFAL adiabatic logic techniques. These 4-bit code converters are shown in figure 4-6 respectively.

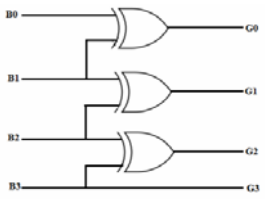

Fig.4. 4-bit Binary to Gray code Converter

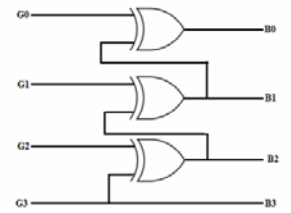

Fig.5. 4-bit Gray to Binary code converter

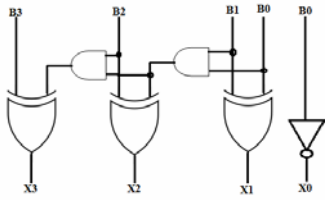

Fig.6. 4-bit Binary to Excess-1 code converter

The designed code converters are implemented with the library of NOT, AND and XOR gates with ECRL and PFAL adiabatic logic. The functionality is verified using Eldo simulator.

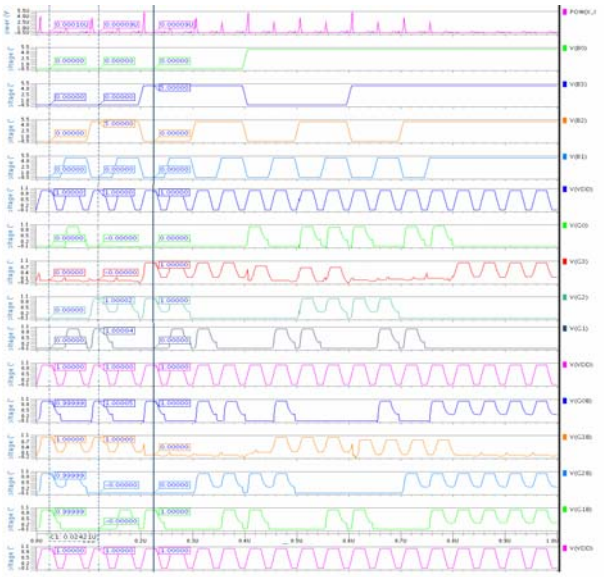

Fig.7.Simulation waveform of 4-bit ECRL Binary to Gray Code Converter

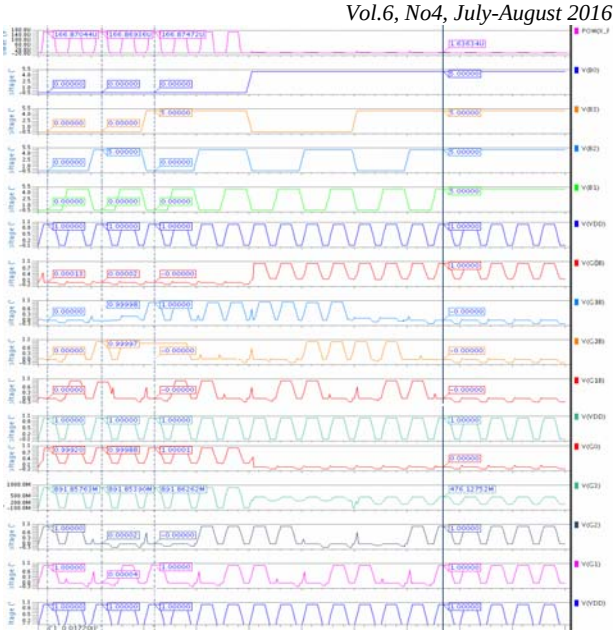

Fig.8.Simulation waveform of 4-bit PFAL Binary to Gray Code Converter

To verify the functionality of adiabatic code converters a trapezoidal power clock with peak to peak amplitude of 5V is taken. The figures 7, 8 show the simulation waveforms of ECRL and PFAL Binary to Gray code converter. The first four waveforms are the input to the code converter. The next four are true and remaining four are the complementary waveforms of the B2G code converter. For the binary input combination of 0100 the true output of gray code is 1100 and the complementary output is 0011. Like this the remaining code converters are also implemented. Further the area and power analysis is carried out in 0.1-100 MHZ frequency range.

IV. RESULTS

The average power dissipation and area are analyzed for the designed circuits and are compared with the CMOS implementation. Table 1 shows the area occupied by designed code converters using CMOS, ECRL AND PFAL logics.

TABLE I

AREA COMPARISON OF CODE CONVERTERS

Code Converter	Area(μm^2)		
	CMOS	ECRL	PFAL
Binary to Gray	13.20	15.68	23.52
Gray to Binary	13.20	15.68	23.52
Binary to Excess-1	18.62	19.6	28.42

TABLE II

AVERAGE POWER DISSIPATION OF BINARY TO GRAY CODE CONVERTER AT DIFFERENT FREQUENCIES

Code Converter	Frequency (MHz)	Power dissipation(μW)	Power saving (%)

		CMOS	ECRL	PFAL	ECRL	PFAL
Binary to Gray	0.1	15.52	6.00	4.086	61	74
	1	40.40	21.90	16.62	46	59
	10	76.27	41.42	34.18	46	55
	100	81.03	60.03	41.79	30	48

TABLE III

AVERAGE POWER DISSIPATION OFGRAY TOBINARY CODE CONVERTER AT DIFFERENT FREQUENCIES

Code Converter	Frequency (MHz)	Power dissipation(µW)			Power saving (%)	
		CMOS	ECRL	PFAL	ECRL	PFAL
Gray to Binary	0.1	8.22	4.91	2.93	40	64
	1	40.42	21.57	18.11	47	55
	10	60.08	52.90	44.00	12	27
	100	82.09	68.90	64.77	16	21

TABLE IV

AVERAGE POWER DISSIPATION OF BINARY TO EXCESS-1 CODE CONVERTER AT DIFFERENT FREQUENCIES

Code Converter	Frequency (MHz)	Power dissipation(µW)			Power saving (%)	
		CMOS	ECRL	PFAL	ECRL	PFAL
Binary to Excess-1	0.1	9.28	5.32	4.73	43	49
	1	41.62	26.61	14.83	37	64
	10	65.99	46.42	43.87	30	34
	100	92.72	71.73	68.06	23	27

The average power dissipation of designed code converters at different frequencies are given in table 2-4. From the power analysis, it is clear that the designed code converters are efficient than CMOS implementations. Among them PFAL achieve more power efficiency.

The following figures show the graphical representation of tables 2-4.

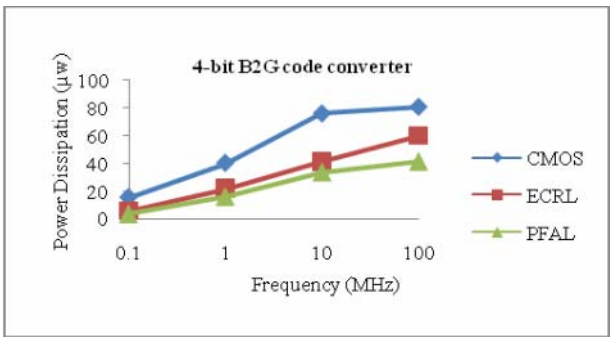

Fig.7. Average power dissipation of Binary to Gray code converter at different frequencies

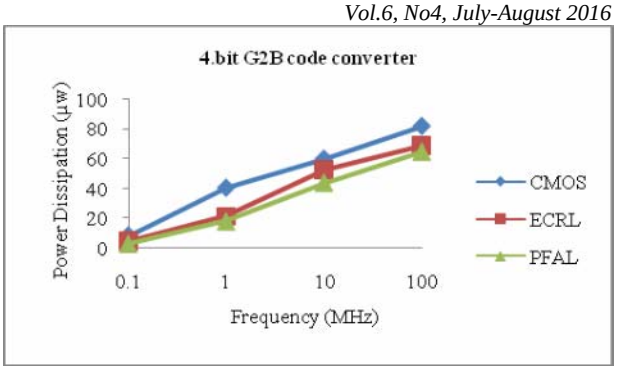

Fig.8. Average power dissipation of Gray to Binary code converter at different frequencies

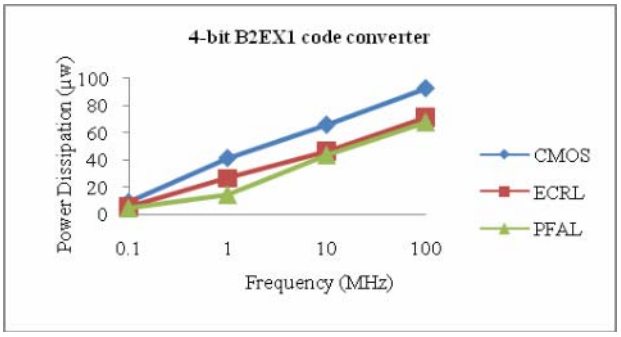

Fig.9. Average power dissipation of binary to excess-1 code converter at different frequencies

V. CONCLUSION

In this paper Binary to Gray, Gray to Binary and Binary to Excess-1 code converters are designed using adiabatic logic techniques at 180nm technology. It is observed that by using the ECRL and PFAL logics the circuit power dissipation is reduced when compared to conventional CMOS logic. The PFAL logic gives more efficiency than ECRL logic at both low and high frequencies.

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