Implementation of Low Power Ultrasonic Phased Array Using ZYNQ-SoC

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***Abstract*—scanning is an art of attain the material properties. Here scanning is performed by sending and receiving the ultrasonic signal. These signals are transmitted using emitter module and then mirrored echo signals are received through receiver module. After acquiring the echo's, they are analyzed with original signal using auto correlation and cross correlation functions, according to changing properties of ultrasonic signal conforming the material like liquid, petrol, sand, solid, etc. This sort of research is usually referred as non-destructive testing. Emitter and Receiver modules are designed in Vivado v2014.4 and are verified on ZYNQ-7000 board; also the received data is analyzed in Matlab 13.1 i.e. high level processing.**

Keywords-emitter module, high level processing receiver module, system on chip (SoC), ultrasonic signal, ZYNQ-7000 board

1. INTRODUCTION

The main empirical of this paper is scanning and, analysis of an object. This work presents a SoC based architecture design, in which ultrasonic phased array analysis is done with airborne transmission. Here macro sequences are derived from complementary set of sequences (CSS) [7].

The received ultrasonic signal contains echoes caused by scattering from grains in materials with a non-homogeneous structure. These echoes are commonly called as backscattering noise. A second source of noise in the ultrasonic signals is noise from electronic circuitry. Ultrasonic phased array [1] has 8-elements and permits the simultaneous scrutiny of 32-different sectors.

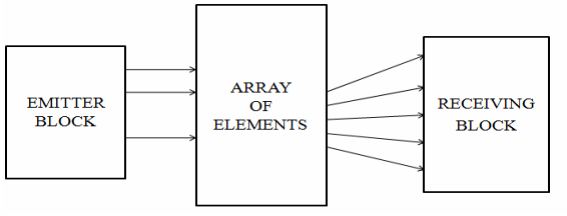

Fig: 1 Main module

The architecture consists of emitter module and receiver module. Both are under the premises of low level processing and then high level processing analyzes the material properties. Fig. 1 shows Main Module of project. Emitter module consist sub blocks i.e. emission control block, BPSK modulator, delay unit. Emission control module continuously generates 12-bit sequences [2]. These sequences are loaded to blocked ram module; 32-sequences are stored in 32-bram modules. These blocked ram module outputs are given as inputs to BPSK modulator. Here 12-bit emission [8] control module output is encoded as 2-bit sequences for reducing the complex operations of BPSK modulator. Emission and reception functional blocks are designed in vivado-14.4. Finally designed architecture is verified on ZYNQ-7000 board and scanning observations i.e. sequences are analyzed in Matlab (high level processing).

BPSK modulator modulates the message signal along with the carrier signal and generates output of 6-bit sequences. These sequences are given as input to delay module and provide 2.47ns delay for each sequence generation. Output of delay module is given as input to summing module; here these sequences are encoded as 12-bit sequences. Emitter has 8-elements these 12-bit sequences are transmitted via emitter elements. These ultrasonic signal can be injected [5] through any material like liquid, solid, sand, petrol etc. and the reflected ultrasonic signal [3] is received by receiver. At the receiver end BPSK de-modulation takes place. De-modulated signal is analyzed and is provided with 1.515ns delay.

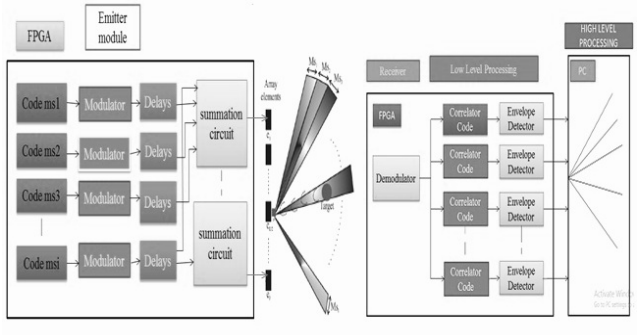

Fig 2 Block diagram of SoC implementation on FPGA

These sequences are then passed to correlator controller module. To ease the analysis, the ultrasonic signal is converted i.e. time domain to frequency domain. As in frequency domain correlation, the mathematical calculations are simple. So we adopt these transformations. For that butterfly architecture is designed. Finally after obtaining 32-different sequences from correlator controller, correlation and comparisons are performed on Matlab. Fig. 2 Block diagram of SoC implementation on FPGA [9]

II. PROPOSED ARCHITECTURE

Here emitter module and receiver modules are implemented on single project, for decreasing the parameters like power and area. This architecture is verified on ZYNQ-7000 board. Results are verified on vivado v2014.4 wave from window. Design consists of emission control block, BPSK modulator, delay unit, summing module BPSK de-modulator, delay unit in receiver, correlator controller all low level processing modules are designed using verilog language. In vivado all project modules are added and also required XDC files and ip's, XDC files are required for I/O planning and ip's required for calling functions like clock, ADC, DAC, etc.

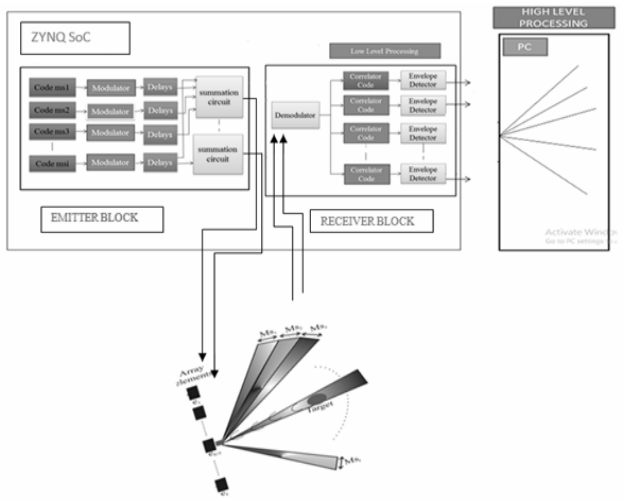

Fig: 3 Block diagram of SoC implementation on ZYNQ-7000 board

Proposed low power ultrasonic phased array design is implemented on single project. Here Fig. 3 shows entire low level processing design and high level processing. This design is verified on ZYNQ-board. Emission control block generated 12-bit sequences stored into code ms1, code ms2, up to code ms32. These blocks are nothing but blocked ram modules (BRAM's). Modulation scheme used in this project is BPSK modulator. Why BPSK modulator? We have ask, fsk, psk, all are digital modulation techniques. Amplitude shift keying (ASK) have high probability error rate P (e) [11] and power consumption parameters. These parameters are more and this modulation scheme is suitable for modem designs. Frequency shift keying(FSK) have parameters probability error rate P(e) is less and power consumption is less but here architecture main them is error free low power design SoC. BPSK modulation have less probability error rate P(e) and less power consumption scheme. This BPSK scheme is best suitable for wireless communication. So BPSK modulation scheme is adapted in our project. Fig. 4 shows the emitter module block diagram.

Emitter module:

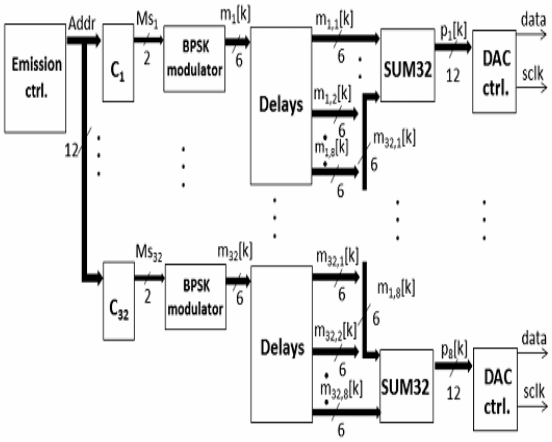

Fig: 4 Emitter module implemented in vivado-14.4

A) Emission Control Block:

This block generates 12-bit sequences continuously they are 000000100000,000000111000, 000001011000 ---------- this sequences nothing but ultra sonic signals in discrete form. Input frequency of this module is 47 MHZ and reset=0 for emitting ultrasonic signal. Baud rate for emission control block is 600Mbps.

B) Blocked Ram (BRAM):

Blocked ram is loaded using output of emission control module. 12-bit sequences are loaded in 32-BRAM modules respectively. These 12-bit sequences are encoded as 2-bit sequences for decreasing complexity of BPSK modulation operation. Here output BRAM module signal is sending to BPSK modulator module. Baud rate of this BRAM module is 100Mbps

C) BPSK modulator:

Blocked ram encoded the message signal that encoded signal is modulated with carrier signal. Here we adopt the digital-communication scheme. So designed BPSK modulator is digital modulator. Carrier signal phase is shifting according to the message signal. Baud rate[4] of BPSK modulator is 300Mbps; 1= no phase shift $0=180^0$ phase shift.

D) Delay module.

Delay module providing 2.47ns delay for sequence generation. After that this sequence is sending to summing module why delay module? Delay module is adopted for decreasing soft-core errors. Baud rate of delay module is 300Mbps.

E) Summing module:

Fig: 5 shows the summing module. Here all sequences are obtained from delay module and 12-bit strengthened signals sequences are generated from delay module. This ultrasonic signal is sending to main emitter module. Clock frequency is 47MHz and reset=0

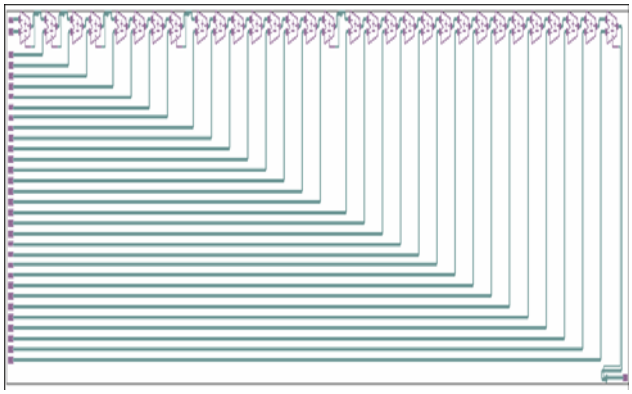

Fig: 5 summing module

F) Digital to analog convertor (DAC):

Digital to analog conversion is performed by calling an IP I.e. DAC_ IP in vivado design. a digital-to-analog converter is a function that converts digital data (usually binary) into an analog signal.

G) Emitter module:

Above all blocks are sub blocks of emitter module. Input of emitter module is 47MHz clock and reset=0, 12-bit strengthened ultrasonic signal is generated from emitter. This ultrasonic signal is inject on any material.eg: solid, liquid, sand, petrol etc. Receiver modules contain following sub blocks i.e. BPSK demodulator, delay unit, correlator controller

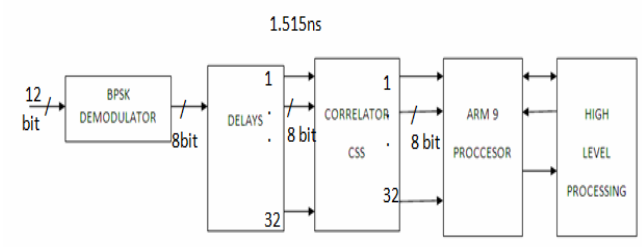

Fig: 6 receiver module block diagram

H) BPSK demodulator:

In this project we adopting modulation technique is coherent modulation. So in this process carrier signal has unique properties. Fig: 6 shows the receiver module block diagram. Input of BPSK demodulator is echo ultrasonic signals i.e. in 12-bit sequence. Demodulation operation is done multiplying carrier with modulated signal

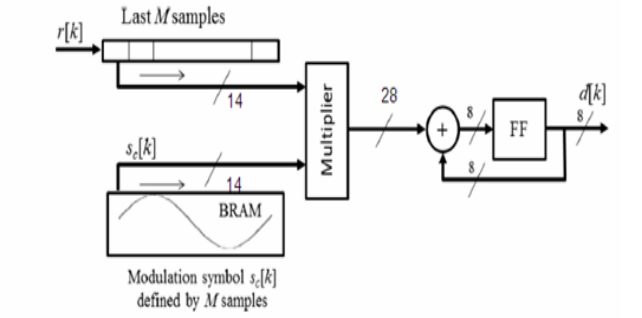

Fig: 7 BPSK demodulator block diagram

Fig. 7 shows the BPSK demodulator block diagram. Normal multiplier operations more compared to booth multiplier so we adopt the booth multiplier in case of BPSK demodulation.14-bit both multiplier is require for performing the BPSK demodulation operation. Generally in VLSI we facing two errors 1.soft core errors 2.hard core errors these errors are optimized using mirror of booth multiplier. In this context booth multiplier and mirror of booth multiplier are designed. Unique Inputs are given to both multipliers. Using comparator comparing the result of both multipliers if Comparator value=0 no errors found if comparator value=1 errors occurred in operation. The soft core and hard core errors are reduced using this technique. Output booth multiplier is 8- bit sequence.

I) Delay unit:

Delay unit is required for controlling the sequence rate. Output of BPSK demodulator is given to the input of delay module. Delay module providing 1.515ns delay. Using this delay control the sequence rate. Output of delay module is given to correlator controller [7].

J) Correlator controller:

Using this controller module converted the time domain signal into frequency domain signal. For that 16 butterfly modules are designed each butterfly module generates 2-outputs I.e. 8-bit sequences. So 16*2=32 sequences are released from this controller. Fig: 8 shows the correlator controller [6].

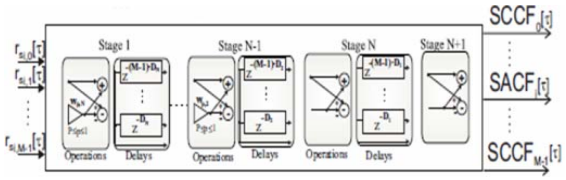

Fig: 8 correlator controller

K) Receiver module:

Above all modules are sub blocks of receiver module. Receiver module input is 12-bit ultrasonic echo signal and clock frequency is 47MHz. output of receiver module is 32---- 8-bit sequences which are stored in ZYNQ board flash memory. Above emitter and receiver modules are under low level processing. Next we going to high level processing.

L) ZYNQ-7000 board:

Emitter and receiver modules are designed in vivado-14.4 and simulation results are verified on simulation window in vivado design suite.

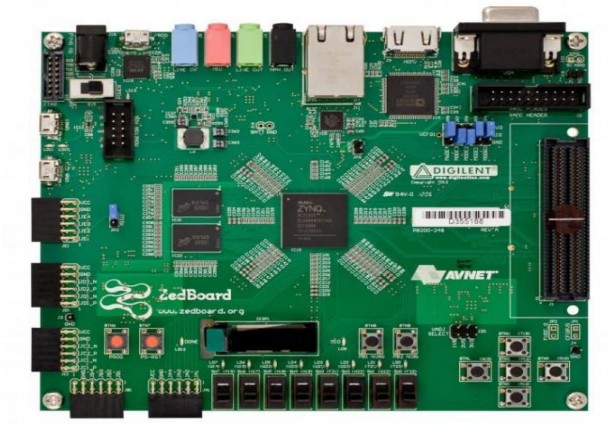

Fig: 9 ZYNQ -7000 Board

M) Analog to digital converter (ADC):

Analog to digital conversion is done in vivado design suite using the IP 'ADC_IP'. After performing the all low level processing operations next we going to high level processing.

N) High level processing:

Using Matlab 13.1 version we are analyzing the output and input sequences. Using auto-correlation and cross-correlation functions observe the properties of material, whether it is solid, liquid, sand, petrol.

III. EXPERIMENTAL RESULTS

Emitter module:

Fig :10(a) Emitter Module

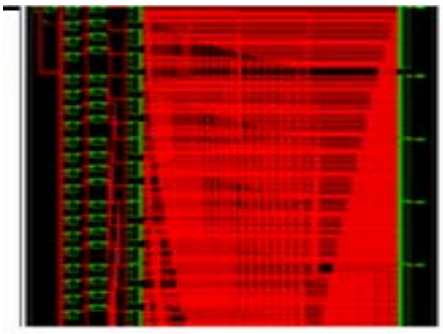

Fig: 10(b) RTL Scematic Of Emitter Module

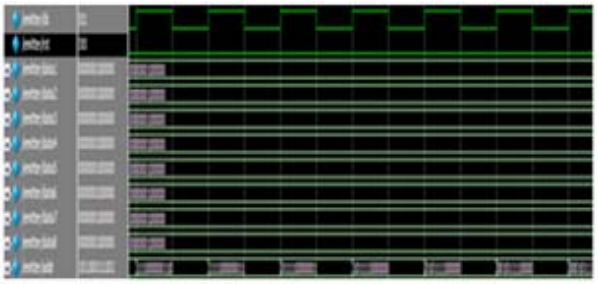

Fig: 10(C) Output Waveforms of Emitter Module

Fig. 10(a) shows the emitter module and Fig. 10(b) shows the RTL schematic of emitter module And Fig. 10(c) shows the output waveforms of emitter module here reset is zero and clock signal is 47 MHz here eight elements are sending 12-bits ultrasonic signals continuously according to emission control block**.**

Receiver module:

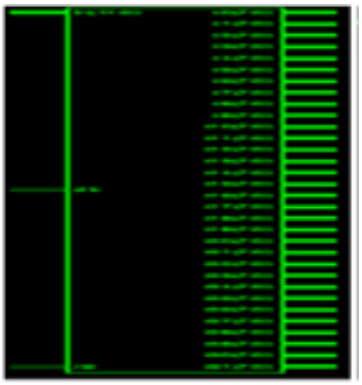

Fig: 11(a) Receiver Module

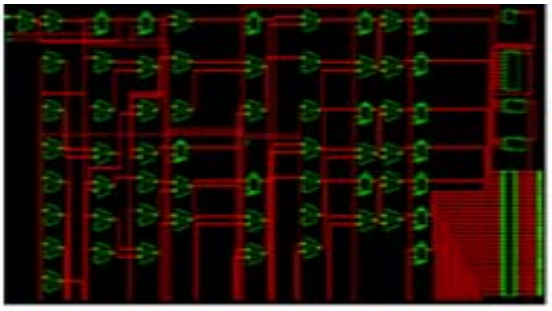

Fig: 11(b) RTL schematic of Receiver Module

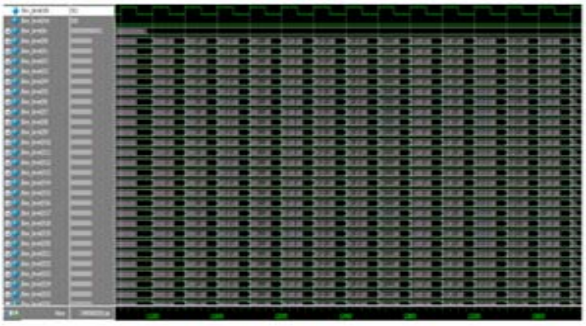

Fig 11(c) output waveforms of receiver module

Fig. 11 (a) shows the output waveforms receiver module and Fig. 11(b) shows the RTL schematic of receiver module and Fig. 11(c) shows the output wave forms receiver module.

Here receiving signal is 12-bit ultrasonic signal and 8-bit sequences generated from controller these signals are in frequency domain.

Main SoC:

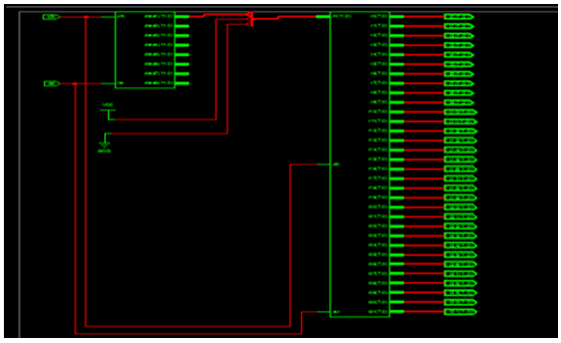

Fig: 12(a) SoC Main Module

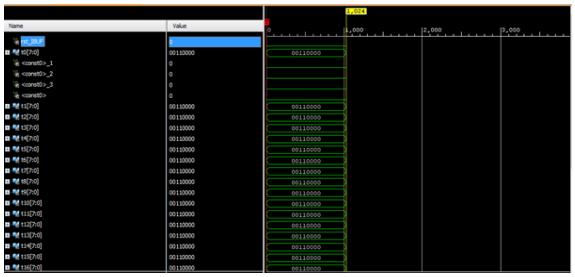

Fig: 12(b) Output Waveforms of SoC

Fig. 12(a) shows the SoC main module here emitter and receiver modules are implemented in single SoC Fig. 12(b) shows the output waveforms of the main SoC module this design is verified on ZYNQ board and simulation results are observed on vivado-14.4 waveform window.

High Level Processing Experimental Results:

Fig: 13(a) when signal doesn't scan any object

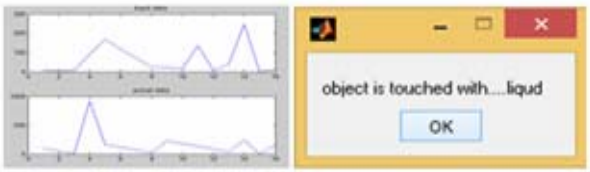

Fig: 13(b) when signal scan liquid

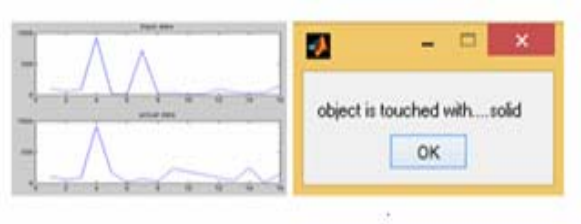

Fig: 13(c) when signal scan solid

Fig: 13(d) when signal scan sand

Fig: 13(e) when signal scan petrol

Above Fig. 13(a) shows when signal doesn't scan any object message is shown as signal is pure. And Fig. 13(b) shows when signal scan liquid, according to correlation values we decide that scanning object is liquid Fig. 13(c) shows when signal scan solid, according to properties of echo signal we decide that scanning object is solid. Fig. 13(d) shows when signal scan sand, according to correlation values and comparing with original ultrasonic signal we decide that scanning object is sand. Fig. 13(e) shows when signal scan petrol According to correlation values, changing properties of ultrasonic signal we decide that scanning object is petrol.

IV. PERFORMANCE ANALYSIS

Table: 1 Power Analysis of SoC design

S No	Design on vertex-6 FPGA	Design on ZYNQ-7000	Percentage power decreasing
1	0.807W	0.204W	74.56%

The proposed method decreases the power up to 74.56%. Due to booth multiplier, modified correlator, and ZYNQ-7000 board. Implementation of SoC design in vertex6 FPGA needs 0.807W same implementation requires 0.204W on ZYNQ board. Table.1 shows the power analysis of SoC design.

V. CONCLUSION

This project allows the simultaneous scanning in particular direction. The proposed architecture can achieve real-time processing, both in the emission and reception of the ultrasonic signals from the proposed phased array. Experimental results are validate, and verified on vivado v 2014.4 and Matlab.

FUTURE SCOPE

This design is very useful in medical applications (scanning area) by increasing the ultrasonic signal strength, Compared to x-rays these ultrasonic scanning reduces the design complexity and cost.

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