A Novel Architecture of 16-Bit Multiplier Using Modified Gate Diffusion Input Logic

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***Abstract*—Multiplication is one of the most an important fundamental function used in digital signal processing. The multiplier plays a vital role in digital signal processing and image processing. The Modified Gate Diffusion Input (MGDI) logic reduces the area of digital circuit while designing the digital circuits. In this paper, Modified Gate Diffusion Input (MGDI) logic technique is used for design of 16-bit multiplier by performing multiplication operation on unsigned numbers. The main modules of 16-bit MGDI multiplier architecture are two's complement generator, Booth encoder, partial product generator, Wallace tree adder and final adder respectively. Reduce in area by using Booth encoding and Wallace tree techniques. They are generate partial products efficiently and well-matched for multiplication of unsigned numbers. Design of 16-bit Multiplier (Radix-4) in Modified Gate Diffusion Input (MGDI) logic requires lesser number of devices as compared to conventional 16-bit Multiplier (Radix-2) design using CMOS and GDI logics. The proposed MGDI designed circuits are extensively simulated on Mentor Graphics tool using AMI 0.5µm CMOS technology.**

***Keywords*—MGDI, Booth Encoder, Partial Product Generator, Wallace Tree Adder.**

I. INTRODUCTION

Design of multiplier using CMOS logic it is occupy substantial area in digital circuits. To further reduce the number of devices in digital multiplier. This can be achieved using a new technique known as Gate Diffusion Input (GDI) logic. Figure 1 shows basic GDI logic cell which is used for implementing complex functions and circuits. Where G, P and N are three inputs and output is taken from D terminal. Which can implement the logic functions are shown in table 1[2]. But this basic Gate Diffusion Input (GDI) logic style having some practical limitations like swing degradation, fabrication complexity in standard CMOS process. These limitations are overcome by Modified Gate Diffusion Input (MGDI) logic. Figure 2 shows basic MGDI cell.

It is contrast with basic GDI cell, MGDI cell contains a low voltage terminal s_p it is connected to a supply voltage and high voltage terminal s_n it is connected to ground.

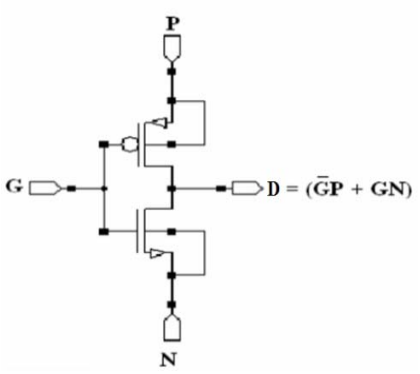

Figure 1: GDI basic cell

TABLE 1: Some functions are implemented in GDI

Inputs			Output
N	P	G	D
'0'	B	A	A'B
B	'1'	A	A'+B
'1'	B	A	A+B
B	'0'	A	AB
C	B	A	A'B+AC
'0'	'1'	A	A'

In the MGDI cell the bulk of PMOS and NMOS are connected to supply voltage and ground with respectively.

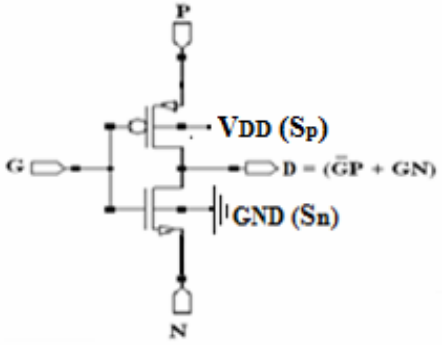

Figure 2: MGDI basic cell

II ARCHITECTURE OF 16-BIT MULTIPLIER

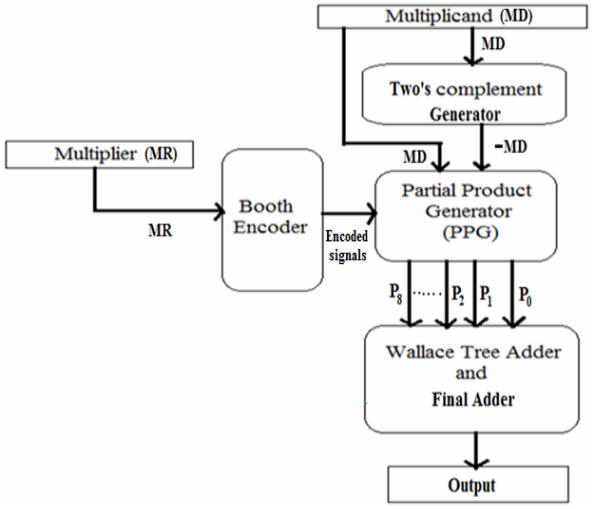

Figure 3: Block diagram of 16-bit MGDI Multiplier

The 16-bit Multiplier Architecture is divided into four modules and each module can be explained in the following subsections.

A. *Two's Complement Generator*

The signed Multiplicand (MD) can be represented in two's complement form, can be obtained by replacing each 1 by 0 and each 0 by 1 of the corresponding Multiplicand bit's, with a 1 added in at the least significant position of the one's complement form.

B. *Booth Encoder*

The Booth encoder is used for reduce the number of partial products based on recoding the Multiplier (MR) in a higher radix. The number, n, of the bits inspected in radix, r, is given by

$$n = 1 + \log_2 r,\ r = 4 \text{ (radix-4)} \qquad (1)$$

$$n = 1 + 2 = 3$$

The Multiplier (MR) can be divided into overlapping groups of three bits at a time this is shown in figure 4.

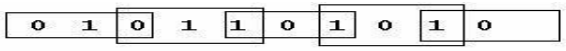

Figure 4: Grouping of triplets from the Multiplier (MR)

By using booth encoder whose functions are given in table 2[5].The operation –MD can be realized by the two's complement of the Multiplicand. The operations 2MD and -2MD can be realized by shifting one bit position of MD and -MD to left and filling the LSB with zero. An easier way to identify the required operation is given by formula is

$$-2d_2 + d_1 + d_0 \qquad (2)$$

TABLE 2: Function Table for Booth Encoder

Input			Function	Encoded Signals			
d2	d1	d0	Fn	neg	two	One	Pos
0	0	0	+0	0	0	0	1
0	0	1	+MD	0	0	1	1
0	1	0	+MD	0	0	1	1
0	1	1	+2MD	0	1	0	1
1	0	0	-2MD	1	1	0	0
1	0	1	-MD	1	0	1	0
1	1	0	-MD	1	0	1	0
1	1	1	-0	1	0	0	0

A simple gate equivalent circuit of booth encoder function table is realized in figure 5.The triplets of Multiplier (MR) are selected at once. Neg, pos signals indicates whether the Multiplicand (MD) is negative or positive. One signal decides to allow the Multiplicand (MD) or it's complementary that is used directly. Two signal indicates whether the left shift operation is to be done on the Multiplicand (MD) or not.

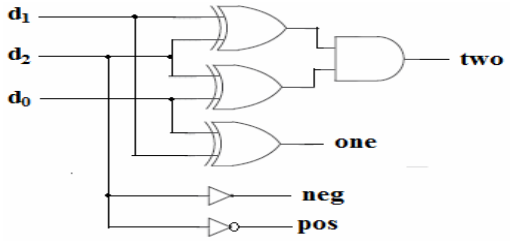

Figure 5: Booth encoder for 3-bit Multiplier (MR)

C. *Partial Product Generator*

The Booth encoder produces the encoded signals. These encoded signals are act as a selection signals which are given to Partial Product Generator. It can be design in number of ways. Here actually used the 2:1 multiplexers for the complete designing of Partial Product Generator. Before design of the Partial Product Generator design the 2:1 multiplexers for the select either the Multiplicand (MD) bits or its complementary bits. Multiplexers are realized using OR and AND gates.

Next design Partial Product generator for 1-bit Multiplicand (MD). It is consists of two 2:1 multiplexers show in figure 6. Where N is operand length, $0 \le i \le (N/2)-1$ and $mdbar_j$ is the complement of md_j,($0 \le j \le N-1$).The first stage of multiplexer unit which has two inputs Multiplicand (MD) and its complement MD bar generated by two's complement Generator.

The neg, pos signals are generated from Modified booth encoder circuit decides to allow the Multiplicand bit or its complementary bit to the next stage. The second

stage of multiplexer which has two inputs two, one signals as only one of the input signal will be high at a time. If two signal is high then it will allow the last state of the input. If one signal is high then it will allow the output from the previous multiplexer to the final output stage.

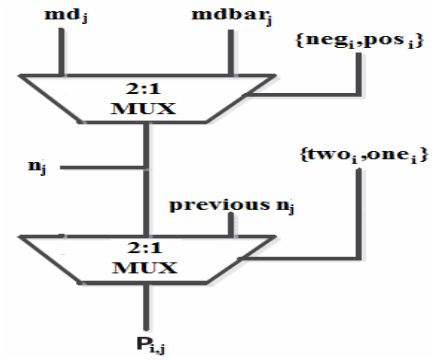

Figure 6: Partial product generator for 1-bit Multiplicand

After generating the partial products and each partial product is a moved two bit position with respect to its neighbors. Next sign extension of each partial product so we can design the sign extension circuits using buffers and inverters by following the processor of template method.

D. Wallace tree adder

After generating the complete partial products are summing by using Wallace tree adder. The Wallace tree adder consists of full adders, half adders and buffers. The partial products are added together by using full adders and half adders then reduce this new matrix and so on, until a two-row matrix is generated such as sum and carry bits. Output of the Wallace tree adder is 32 bits sum and 32 bits carry.

E. Final adder

The Wallace tree adder generates the 32 bits sum and 32 bits carry. Finally sum and carry get summed up with a final adder. The final adder consists of full adders, buffers. Output of the final adder is 32 bits multiplied output.

The Finally figure 7, shows the dot diagram of 16-bit Multiplication using Radix-4 Booth algorithm.

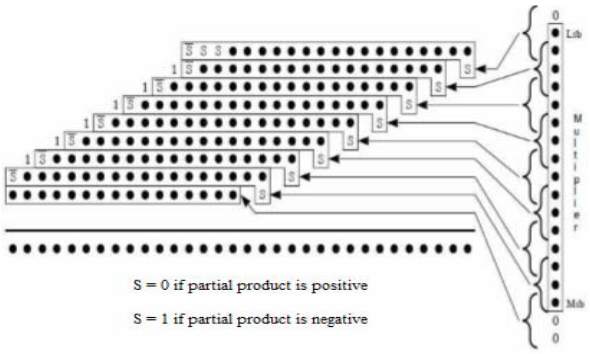

Figure 7: Dot diagram for 16-bit Multiplication

III IMPLEMENTATION OF 16-BIT MULTIPLIER USING MGDI

The 16-bit Multiplier shown in figure 3 is now designed using MGDI logic using Mentor Graphics tool using AMI 0.5 µm CMOS technology at 2.5v supply voltage.

In the first step, design of basic gates, main modules like two's complement generator, partial product generator and sub modules like full adders, half adders are carried out in MGDI. These sub modules are combined in the main modules of 16-bit Multiplier design.

Design of basic gates (AND, OR) and XOR gates in MGDI logic:

The two input AND & OR gates are implemented in Modified Gate Diffusion Input (MGDI) logic and to avoid the swing degradation. The schematic of these gates are shown in figure 8 & figure 9 respectively [2]. Inverters are used for the complement of inputs. Buffers are in build of inverters and to improve ability of outputs. Also, XOR gate realized as shown in figure 10.

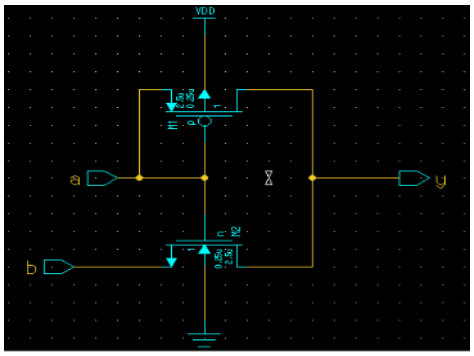

Figure 8: Schematic of two input MGDI AND gate

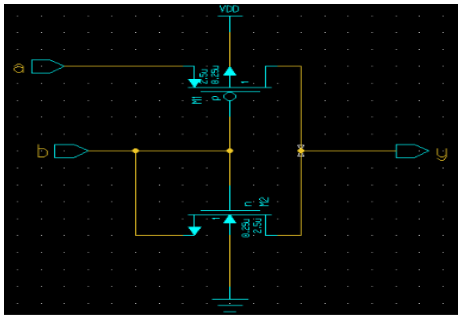

Figure 9: Schematic of two input MGDI OR gate

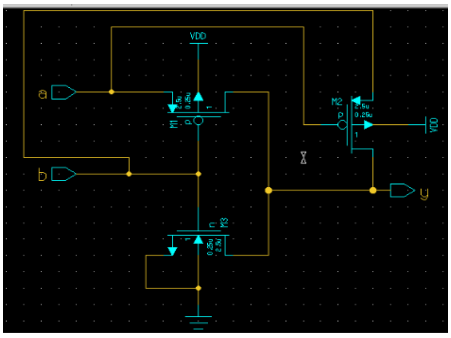

Figure 10: Schematic of two input MGDI XOR gate

The sub modules are designed by using above gates. Like half adder is implemented as sum, carry using XOR gate and AND gate respectively. Full adder is implemented as sum, carry using XOR gate, inverter and two transistors of two 2:1 multiplexers shown in figure 11.

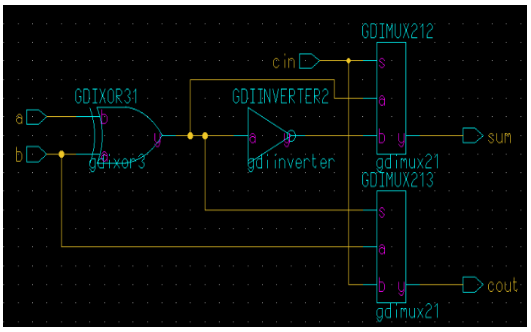

Figure 11: Schematic of MGDI Full adder

The design of 16-bit Multiplier is made by combining these sub modules to improve the main modules such as Booth encoder, Two's complement generator, Partial product generator, Wallace tree adder and Final adder. The schematic of these main modules are as shown in figure 12, figure 13 and figure 14.

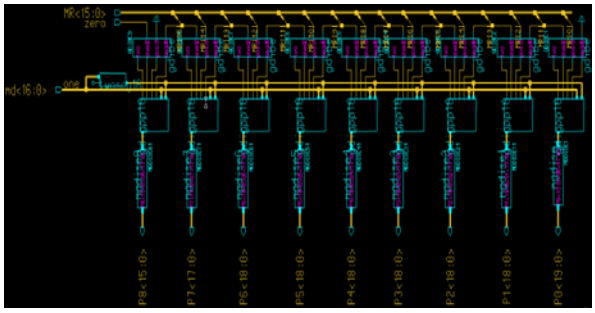

Figure 12: Schematic of Partial product generator along with Booth encoder and Two's complement generator

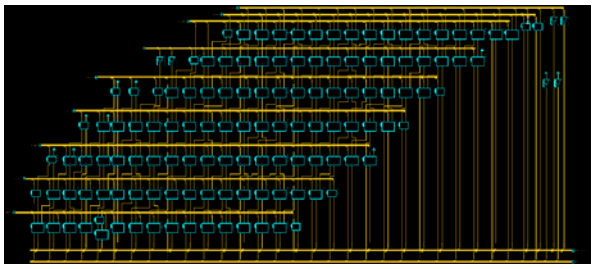

Figure 13: Schematic of MGDI Wallace tree adder

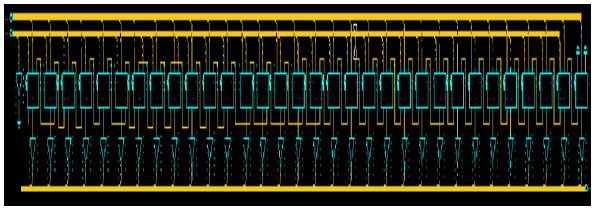

Figure 14: Schematic of MGDI Final adder

The final 16-bit Multiplier is implemented by using combining the main modules as indicated in figure 3. The final schematic of 16-bit Multiplier is shown in figure 15.

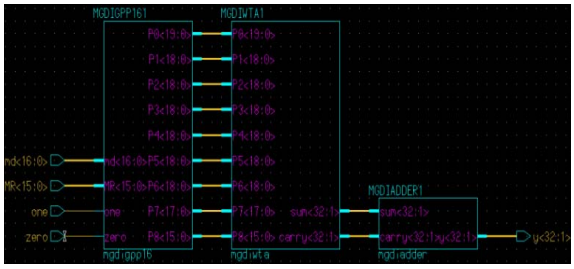

Figure 15: Schematic of Final 16-bit MGDI Multiplier

IV SIMULATION RESULTS AND COMPARATIVE STUDY OF THE 16-BIT MULTIPLIER DESIGN

The Schematic of Multiplier is designed using Mentor Graphics tool using AMI 0.5 µm CMOS technology at 2.5v supply voltage. The W/L ratio of both pMOS and nMOS transistors are taken as 2.5/0.25µm and simulation is done for 16-bit multiplication, figure 16 shows simulation results for input Multiplicand $(45671)_{10} = (0101100100110011)_2$ and Multiplier $(38503)_{10} = (1001011001100111)_2$ and its Multiplied output is $(1758470513)_{10} = (01101000110100000010000101110001)_2$.

The comparative study of design of Multiplier is made with reference to the number of devices required for 16-bit Multiplier in CMOS, GDI and MGDI designs. Shown in table 3 indicates number of devices required to improve the basic gates and adders in CMOS, GDI and MGDI logics.

TABLE 3: Comparison of No. of devices required to improve the basic gates and adders in CMOS, GDI and MGDI logic styles.

Sl. No.	Gates/Adders	Devices in CMOS	Devices in GDI	Devices in MGDI
1	Inverter	2	2	2
2	Two input AND Gate	6	5	2
3	Two input XOR Gate	12	8	3
4	Two input OR Gate	6	4	2
5	Half Adder	18	13	5
6	Full Adder	42	32	9

The requirement of pMOS and nMOS devices for main modules of conventional 16-bit Multiplier (Radix-2) is implemented by using CMOS and GDI logics shown in table 4. Here the conventional final 16-bit Multiplier (Radix-2) had some drawbacks such as

1. It is creates a larger number of partial products and allow the partial product summation to be slowly and use more hardware.
2. It is becomes inefficient when there are isolated 1's.

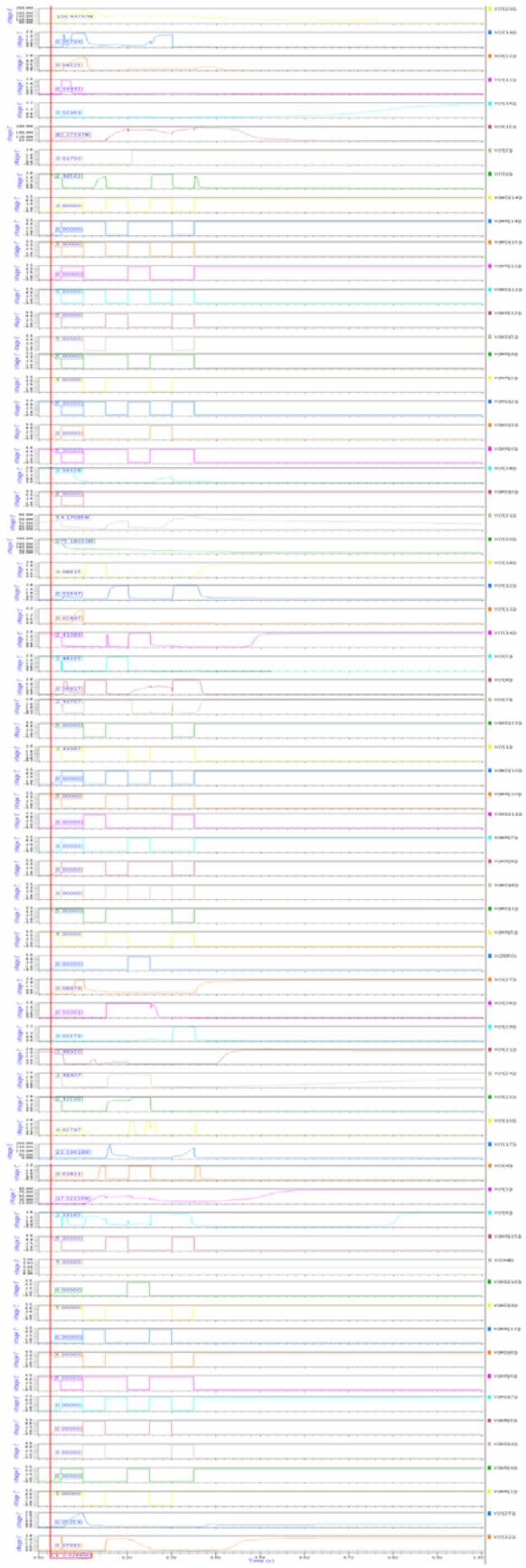

Figure 16: Simulation waveforms of 16-bit MGDI Multiplier

TABLE 4: Requirement of number of devices required to implement main modules of 16-bit Multiplier (Radix-2) in CMOS and GDI logics.

Sl. No.	Main Modules	Number of devices in CMOS design	Number of devices in GDI Design
1	Two's complement generator	320	240
2	Booth encoder	318	238
3	Complete partial product generator	9888	8864
4	Adder circuit	14740	11220
5	Final 16-bit Multiplier	25266	20562

These problems are overcome by using Modified Booth Algorithm (Radix-4) which scans triplets of Multiplier (MR).

It is creates a smaller number of partial products and allow the partial product summation to be faster and use less hardware by using Booth encoding and Wallace tree technique. The requirement of pMOS and nMOS devices for main modules of final 16-bit Multiplier (Radix-4) is implemented by using MGDI logic shown in table 5.

TABLE 5: Requirement of number of devices required to implement main modules of 16-bit Multiplier (Radix-4) in MGDI logics.

Sl. No.	Main Modules	Number of devices in MGDI Design
1	Two's complement generator	119
2	Booth encoder	153
3	Complete partial product generator	2808
4	Adder circuit	1536
5	Final 16-bit Multiplier	4344

II. Conclusion

The 16-bit Multiplier is designed in MGDI logic with Booth encoding and Wallace tree addition techniques using Mentor Graphics tool. The objective of Multiplier is design in MGDI is to show reduction of area in the Multiplier design compared to CMOS and GDI designs. A comparative study is made regarding the total number of devices required for the Multiplier design using CMOS, GDI and MGDI logics. It is observed that Multiplier designed in MGDI results in reduction of devices, thus minimizing the area of Multiplier.

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