

# Performance Analysis of High Performance Energy Efficient Logic Styles in VLSI

Viya Vijayan

PG Scholar, VLSI and Embedded Systems  
St. Joseph's College of Engineering and Technology  
Palai, Kerala, India  
[viyavijayan@gmail.com](mailto:viyavijayan@gmail.com)

Sunitha S Pillai

Asst.Prof.,ECE Department  
St. Joseph's College of Engineering and Technology  
Palai, Kerala, India  
[sunithapillai2005@yahoo.co.in](mailto:sunithapillai2005@yahoo.co.in)

**Abstract**— This paper presents a comparative study of high performance energy efficient logic styles in VLSI circuits. It has a keen role in the field of VLSI circuits. As the VLSI technology is upgrading this energy efficient logic styles are also upgrading. This logic styles include dynamic domino logic in earlier then followed the FTL. Later uses the CD (constant Delay) logic style as most recent logic style. This paper concentrated on the CD logic style which has the advantage of speed and performance over the other logic style. Simulation result illustrates the implementation of simple AND gate in different logic style and its comparison based on its speed, delay and performance. The implementation was carried out in Mentor Graphics IC Station.

**Keywords**- High performance logic style, FTL, Constant Delay, VLSI.

## I. INTRODUCTION

The integrated circuits(IC) has vital role in today's world as it posses the realization of virtually all electronics circuits that might be unthinkable a few years back. This is Thanks to Moore's Law [1]. Moore's law is the basis for all VLSI technologies; the most important process that this law carried out is the scaling down of CMOS device. However it having some disadvantage; it may possess high density and performance.

VLSI technology includes many of the logics in which high performance energy efficient logic style has always been a great research area. All the logic styles can be rated in the basis of its digital design performance merits. The digital design performance merits is the key factor for analysis purpose of the logic styles. This Include;

- Delay
- Power dissipation

Delay is the most important performance merit of the digital design. Delay can predict the speed of the system and hence

the operating frequency. Mainly the delay stands for propagation delay. It can be defined as the average of the response time from low to high transition and vice versa [2].

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \quad (1.1)$$

Power dissipation is also an important design merits for the high performance energy efficient logic style. It gives the amount of power consumed by digital circuits under the specified conditions. Power dissipation includes dynamic power dissipation as well as the static power dissipation. Dynamic power consumption can be defined as the amount of energy requires a transistor to charge or discharge the capacitor. It can be given by;

$$P_{dynamic} = C_L V_{DD}^2 f_{switch} \quad (1.2)$$

$f_{switch}$  in equation (1.2) denotes the number of times a device switched per second;  $V_{DD}$  is the supply voltage;  $C_L$  is the energy stored. Static power consumption can be given by:

$$P_{static} = I_{static} V_{DD} = I_{leakage} V_{DD} \quad (1.3)$$

Equation (1.3) is used to find the power dissipation caused by leakage current etc [3]. Involving this design merits the era of energy efficient logic styles had been started from 1980's with dynamic domino logic[4]. But it gradually lost the performance because of high self loading. By the result of a significant research, a new way of logic operation is invented; known, as feed through logic [5]. In recent years a better logic called constant delay (CD) than FTL is invented by the designers and

this logic is now widespread in the VLSI technology. This paper is also concentrated in constant delay logic style.

This paper is organized as follows; section II is dealing with the basic energy efficient logic style domino logic. Section III carries the concept of feed through logic (FTL).Constant delay logic style is explained in detail in section IV .Section V composed of simulation result an analysis. Conclusion is given by section VI.

## II. DYNAMIC DOMINO LOGIC

Dynamic domino logic has been invented in the beginning of 1980s.Using this logic designer could have been implemented the ALU circuit block. Domino circuit composed of PDN chain, CMOS and not gate. Figure 1 shows the circuit diagram for dynamic circuit and working of dynamic circuits as follows;

During the pre-charge phase CLK is 0; all output nodes all (N') of the dynamic gates are pre-charged to high via transistor MP, and thus the outputs (N) of the corresponding buffers are pre-charged to low. Since all transistors of subsequent dynamic gates are fed from such buffers, these will be turned off during the pre-charge phase. During the evaluation phase, nodes N' are either discharged through transistor MN or they remain high. So the outputs N of the buffers either go to high or remain low, respectively [4]. But this dynamic circuits having some disadvantage like charge sharing problem and high power dissipation due to data activity.

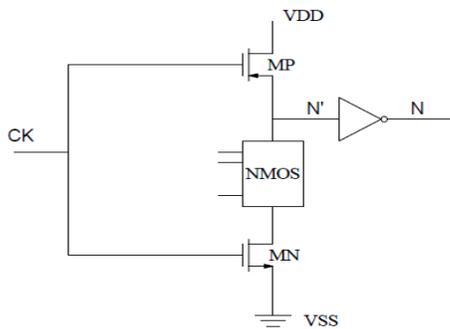


Figure1.Dynamic domino logic.

## III. FEED THROUGH LOGIC(FTL)

New way of logic style, also known as feed through logic, which overcome the disadvantage of dynamic domino logic has been proposed [5]. It works on the domino concept; with the added feature that gates commence evaluation even before their inputs are valid. It results in very fast computational

blocks [6].Figure 2 shows the diagrammatic representation for the feed through logic.

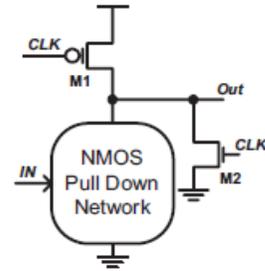


Figure2.Feed through logic

The operation of FTL is given as follows; when CLK is enable(logic 1), start the pre discharge period and Out is pulled down to GND via M2. When CLK becomes low, M2 is off, while M1 is on and the gate enters the evaluation period at the same time. If an input (IN) is 1, Out going to the contention mode meanwhile M1 and transistors in the NMOS pull-down network (PDN) are conducting current simultaneously. When PDN is off, then the output quickly rises to logic "1." For this case, the critical path is always a single PMOS transistor. Feed through logic has some disadvantage of reduced noise margin and power dissipation.

## IV. CONSTANT DELAY LOGIC

Constant delay logic is proposed in [7].It has very important row in VLSI energy efficient circuits due to its low power dissipation. Constant delay logic composed of;

- Timing block(TB)
- Logic Block(LB)

Timing block creates the adjustable window period to nullify the static power dissipation while logic block reduce the glitches posses in the output section and makes possible cascading CD logic. Figure 3 shows the simple buffer circuit with CD logic and its operation as follows;

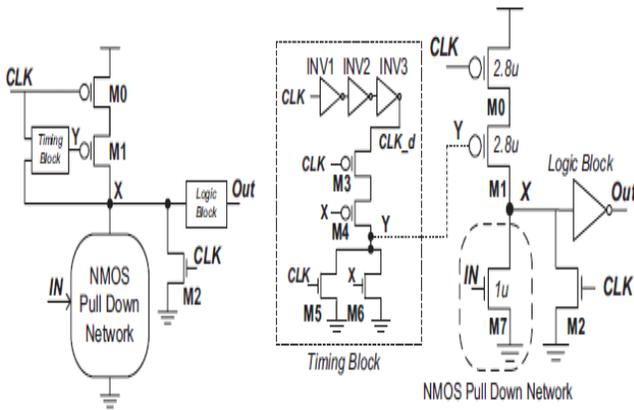


Figure3.Constant delay logic.

The input to the CD logic is from dynamic logic gate. When CLK is high, the CD logic enters into the discharge state and the point X, Y pull down to ground. When CLK become low, the CD goes to the evaluation period, this evaluation period consisting of three modes of action;

- Contention mode
- C-Q delay
- D-Q delay

These three modes of operation can explain with the help of timing diagram given in figure 4 [7].

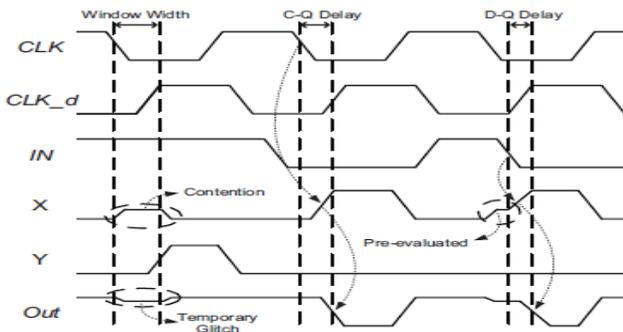


Figure4.Timing diagram of CD logic.

During contention mode, CLK is low and input will be 1, X will be in a non zero voltage level. The output experiences a temporary glitch only. The contention period is over when M1 transistor become off. In C-Q delay mode the input gets high to low transition, then only the CLK become low. When CLK become 0, X → 1, Y → 0, for entire evaluation period. Delay can be calculated by the falling edge of both CLK and OUT; hence the name C-Q delay. D-Q delay mode utilizes the pre-evaluated characteristics of CD logic to enable the high

performance. In this mode the CLK getting high to low transition before the IN transit. When IN is 0 and Y is 0 then the X goes 1. A race condition is exist between X and Y. The summary of CD logic is given in the table 1 [7].

Mode	Scenario	Operation
Pre-discharge	CLK is high	X and Out are pre-discharged and pre-charged to GND and VDD, respectively
Contention	IN = "1" for the entire evaluation period	Direct path current flows from PMOS to PDN. X rises to a nonzero voltage level and Out experiences a temporary glitch
C-Q Delay	IN goes to "0" before CLK transits to low	X rises to logic "1" and Out is discharged to VDD. Delay is measured from CLK to Out
D-Q delay	IN goes to "0" after CLK transits to low (while window is still open, i.e., Y is still "0")	X initially enters contention mode and later rises to Logic"1." Delay is measured from IN to Out

Table1. Summary of CD logic.

## V. SIMULATION RESULTS AND ANALYSIS

The simulation is carried out using Mentor Graphics IC station .A simple AND gate with dynamic domino logic, FTL and CD logic are used for the simulation purpose. Moreover done a comparison between these energy efficient logic style based on power consumption and delay. Circuit design and simulated waveforms in different logic style is given below.

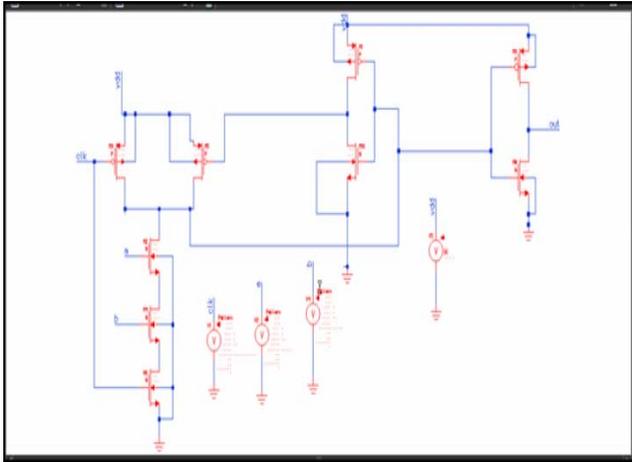


Figure5.circuit diagram for dynamic domino logic

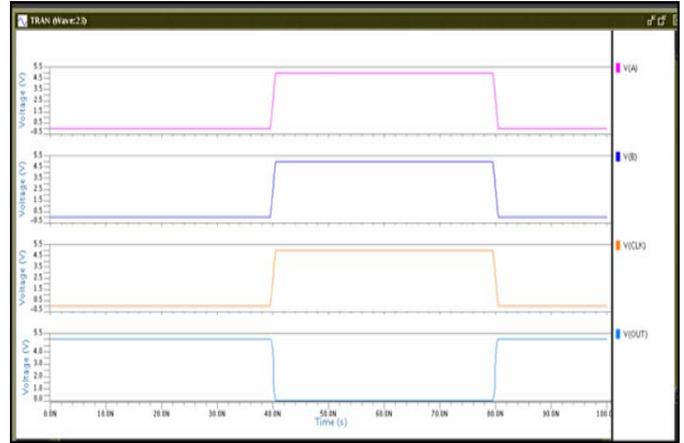


Figure8.waveform of feed through logic

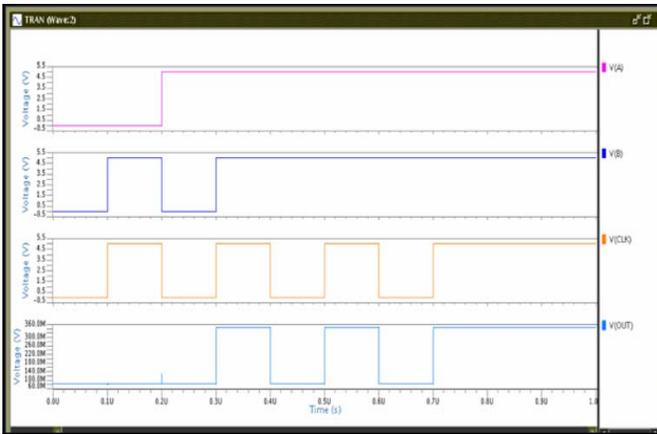


Figure6.waveform of dynamic logic

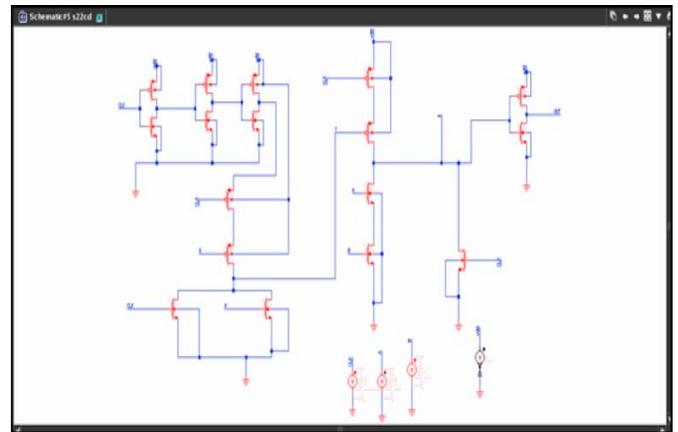


Figure9.Circuit diagram for Constant Delay logic

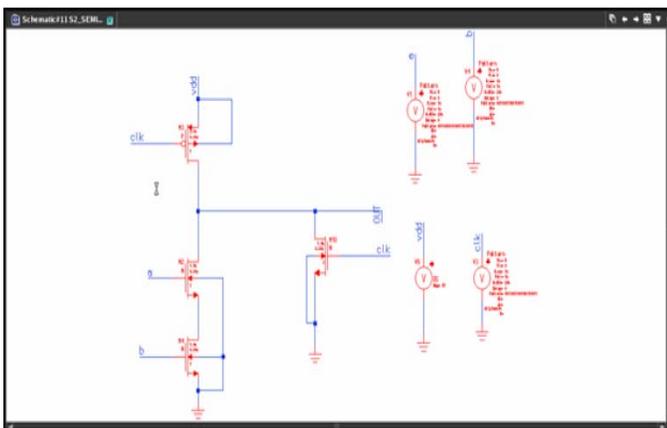


Figure7.Circuit diagram of feed through logic

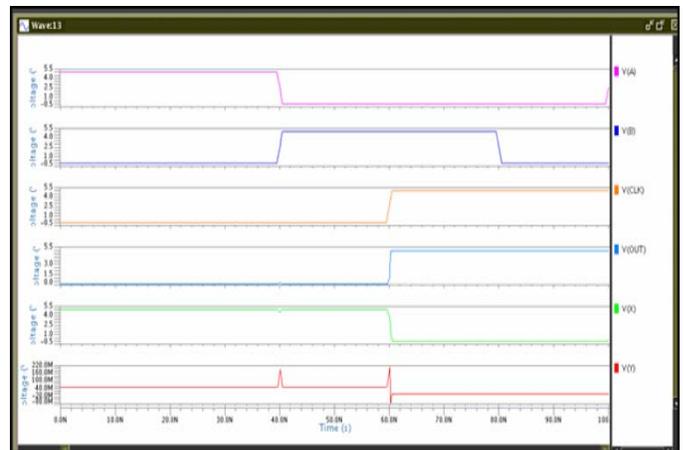


Figure10.Waveform of Constant delay logic.

Delay and power consumption of each logic style is listed in the table below.

Logic style	Power consumption	Delay
Dynamic domino logic	296.1080uW	392.254uS
Feed through logic	244.355nW	425.875nS
Constant delay	234.15pW	541.254pS

## VI. CONCLUSION

We have presented performance analysis of energy efficient logic styles regarding power consumption and delay in this paper. The experiment was carried using the tool Mentor Graphics IC. Three logic style namely dynamic domino logic, feed through and constant delay are considered in this paper. We could conclude that constant delay logic is more energy efficient logic style than other two and it is wide spread.

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## AUTHORS PROFILE

**Ms.Sunitha S Pillai:** received the Bachelors degree in Electronics and Communication from College of Engineering, Perumon. She received his Masters degree from National Institute Of Technology, Surathkal. She is working as an Assistant Professor for the last eight years in the Department of Electronics and Communication at St. Joseph's College of Engineering and Technology, Palai.

**Miss.Viya Vijayan:** received the Bachelors degree in Electronics and Communication from Ilahia college of engineering and Technology, Muvattupuzha affiliated to Mahatma Gandhi University, Kottayam in 2012. Presently she is doing M.Tech in VLSI and Embedded Systems from St. Joseph's College of Engineering and Technology, Palai.